

MOS-Mobility

Effect of Process Variations on 4H Silicon Carbide MOSFET Mobility

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Improved Channel Mobility in Normally-Off 4H-SiC MOSFETs with Buried Channel Structure

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Channel Engineering of Buried-channel 4H-SiC MOSFET Based on the Mobility Model of the Oxide/4H-SiC Interface

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4H-SiC MOSFETs on (03-38) Face

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MISiCFET Chemical Gas Sensors for High Temperature and Corrosive Environment Applications

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4H-SiC Material for Hall and Effect and High Temperature Sensors Working in Harsh Environment

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**High Temperature Performance of 10 Kilovolts, (Late News) 200 Amperes (Pulsed)
4H-SiC PiN Rectifiers**

R. Singh, K. G. Irvine, J. T. Richmond, J. W. Palmour

Cree Inc., USA

Effect of Process Variations on 4H Silicon Carbide MOSFET Mobility

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The critical field for avalanche breakdown in SiC is about 10x higher than in silicon, so SiC unipolar power devices are theoretically capable of specific on-resistances about 400x lower than silicon devices. However, the on-resistance of 4H-SiC power MOSFETs reported to date has been limited by the resistance of the MOS channel, and not by the drift region. This is because of the low electron mobility in SiC inversion layers. Recently it has been shown that a post-oxidation anneal in nitric oxide (NO) can significantly reduce the interface state density in the upper half of the bandgap, with a corresponding improvement in mobility [1]. To determine the effect of processing variables on MOSFET mobility in 4H-SiC, we have conducted a comprehensive set of experiments that will be reported here.

Figure 1 illustrates the matrix of experimental conditions. The experiment consists of the following comparisons: (1) S/D implant anneal (1200 C or 1400 C), (2) oxidation procedure (Auburn or Purdue), (3) post-oxidation anneal (none or NO), (4) gate material (polysilicon or molybdenum), and (5) ohmic contact anneal (before and after). Nine samples are reported here. Samples A - F are fabricated on the same p-type epilayer wafer and oxidized at Auburn, while W - Z are fabricated on a second p-type epilayer wafer and oxidized at Purdue.

Figure 2 shows drain current vs. gate voltage for eight samples, with and without a post-oxidation anneal in nitric oxide (NO) at 1175 C for 120 min. The post-oxidation anneal in NO produces an order of magnitude higher drain current in all samples. Figures 3 and 4 show field-effect mobility μ_{FE} of samples oxidized at Auburn *with* (B, F) and *without* (A, E) the post-oxidation NO anneal. Suffixes (a) and (b) denote these samples *before* (b) and *after* (a) an 850 C ohmic contact anneal. The NO anneal produces a dramatic increase in field-effect mobility. The 1400 C implant anneal (E, F) does not significantly degrade the mobility as compared to the 1200 C anneal (A, B), and the ohmic contact anneal likewise has little effect on mobility. Figure 5 shows that the choice of gate material also has little effect.

Figures 6 and 7 show similar results for samples oxidized at Purdue. Suffixes (a) and (b) denote these samples *before* (b) and *after* (a) a 770 C ohmic contact anneal. The mobilities are slightly higher for the Purdue samples as compared to the Auburn samples, due possibly to slight differences in oxidation procedure. Since these are field-effect mobilities (as compared to effective mobilities), the drain current is proportional to the *integral* of μ_{FE} with respect to gate voltage. As shown in Fig. 8, samples W and X carry slightly higher drain current than B and F, even though at gate voltages of 20 V the mobilities are comparable.

Details of the oxidation and anneal procedures will be reported at the conference. Mobility measurements are performed by a new "constant current" technique that eliminates the effect of source and drain resistances. This technique will also be described at the conference.

This work is supported by ONR MURI grant N00014-95-1-1302 (Purdue) and by DARPA/EPRI grant MDA972-98-1-0007/W08069-05 (Auburn and Vanderbilt).

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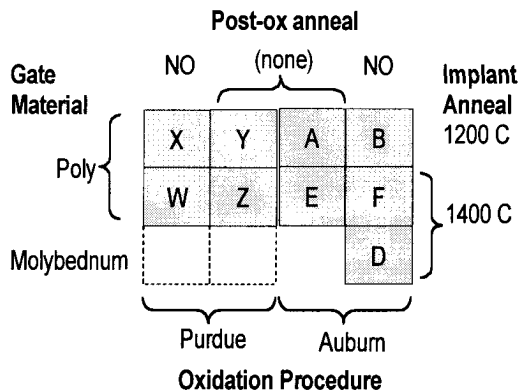


Fig. 1. Matrix of experimental conditions. Letters A - F identify samples oxidized at Auburn and W - Z designate samples oxidized at Purdue.

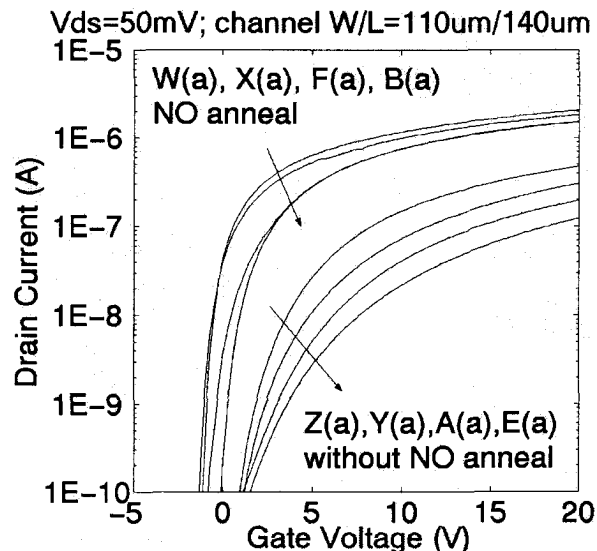


Fig. 2. Drain current vs. gate voltage for samples with a post-oxidation anneal in NO (upper curves) and without (lower curves).

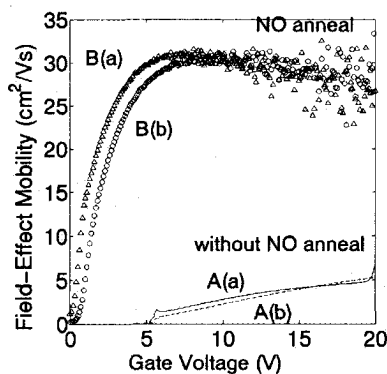


Fig. 3. 1200 C implant anneal, AU oxide, before (b) and after (a) an 850 C contact anneal.

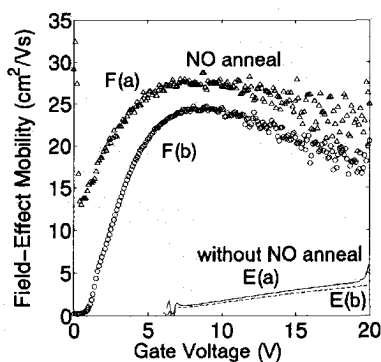


Fig. 4. 1400 C implant anneal, AU oxide, before (b) and after (a) an 850 C contact anneal.

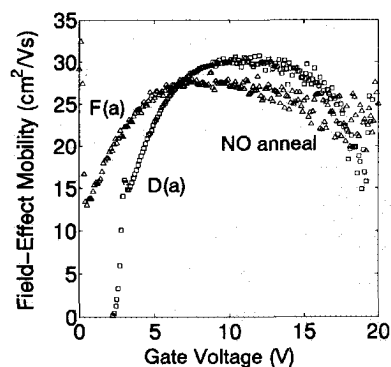


Fig. 5. 1400 C implant anneal, AU oxide, polysilicon gates (F) and molybdenum gates (D).

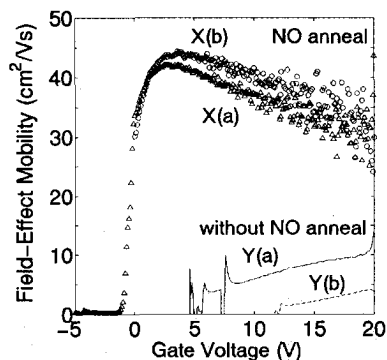


Fig. 6. 1200 C implant anneal, PU oxide, before (b) and after (a) a 770 C contact anneal.

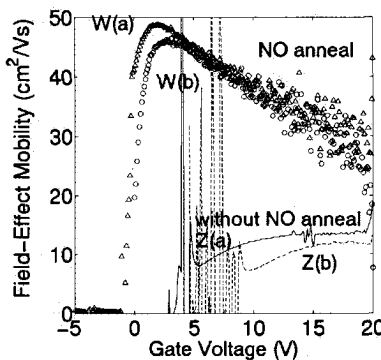


Fig. 7. 1400 C implant anneal, PU oxide, before (b) and after (a) a 770 C contact anneal.

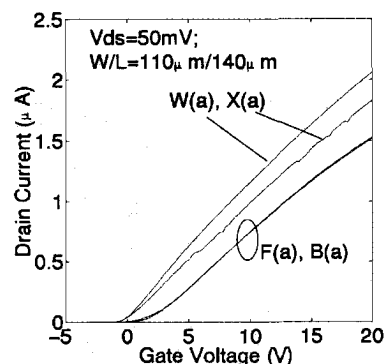


Fig. 8. Drain current at a drain voltage of 50 mV for samples W, X, F, and B of Fig. 2.

Improved Channel Mobility in Normally-off 4H-SiC MOSFETs with Buried Channel StructureS. Harada^{1,2}, S. Suzuki^{1,3}, J. Senzaki^{1,2}, R. Kosugi^{1,2}, K. Fukuda^{1,2}, and K. Arai^{1,2}¹Ultra-Low-Loss Power Device Technologies Research Body²Power Electronics Center, National Institute of Advanced Industrial Science and Technology³R&D Association for Future Electron Devices

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4H-SiC metal-oxide-semiconductor field effect transistor (MOSFET) is a promising candidate for a high-power switching device. The most important problem for this device is to improve the channel mobility in the inversion layer. The reported channel mobility until now is extremely lower than the bulk electron mobility [1, 2]. It is generally believed that high density of interface traps at the SiO₂/4H-SiC interface degrades the channel mobility [3, 4]. One possible solution for the improvement of the channel mobility is to utilize the buried channel structure. In this structure, more electrons can flow away from the MOS interface. Therefore, the channel mobility may be significantly improved in 4H-SiC MOSFET. In this study, we have fabricated the buried channel MOSFETs on 4H-SiC. Oxidation conditions for the gate oxide and the doping depth of the buried channel region were optimized. The channel mobility of 140 cm²/Vs was achieved in the normally-off 4H-SiC MOSFET.

The buried channel MOSFETs were fabricated on the p-type 4H-SiC (0001) wafer with an effective doping concentration ($N_A - N_D$) of approximately 5×10^{15} cm⁻³. Figure 1 shows structural cross section of the MOSFET. The channel length and width were 100 and 150 μ m, respectively. The buried channel region was formed by nitrogen ion implantation at room temperature and following activation annealing at 1500 °C. The nitrogen concentration was 1×10^{17} cm⁻³, and the depth of the buried channel region (D_{ch}) after the gate oxidation were 0.15, 0.20, 0.25 μ m. The gate oxide was grown by dry or wet oxidation at 1200 °C and following Ar annealing at the oxidation temperature. Some samples were then subjected to a wet re-oxidation at 950 °C for 3 hours. Aluminum was deposited as the gate and the source/drain contacts.

Figure 2 shows field effect mobility (μ_{FE}) as a function of gate voltage for the buried channel MOSFETs with the gate oxide processed by different condition. Drain voltage for this measurement was 0.1 V. The peak values are much higher than those in the inversion-type 4H-SiC MOSFET [5], indicating that the channel mobility is significantly improved by the buried channel structure. Threshold voltage (V_{th}) was extracted from $I_D^{1/2}$ - V_G plot at $V_D=10$ V. Wet, dry/wet and wet/wet oxidation samples have positive V_{th} due to the normally-off operation. The highest μ_{FE} in the normally-off MOSFET is 140 cm²/Vs for the gate oxide prepared by the dry/wet oxidation. Figure 3 shows the μ_{FE} as a function of gate voltage and D_{ch} . The gate oxide was formed by the dry/wet oxidation. The peak values for the D_{ch} of 0.15, 0.20, and 0.25 μ m are 45, 140, and 230 cm²/Vs, respectively. The V_{th} for the D_{ch} of 0.15 and 0.20 μ m are positive values. These results reveal that the optimum D_{ch} for the normally-off buried channel MOSFET is 0.2 μ m when the doping concentration is 1×10^{17} cm⁻³. The channel mobility of 140 cm²/Vs is the highest reported so far for normally-off 4H-SiC MOSFETs with a thermally grown gate oxide.

This work was performed under the management of FED as a part of the METI New Sun Shine Program (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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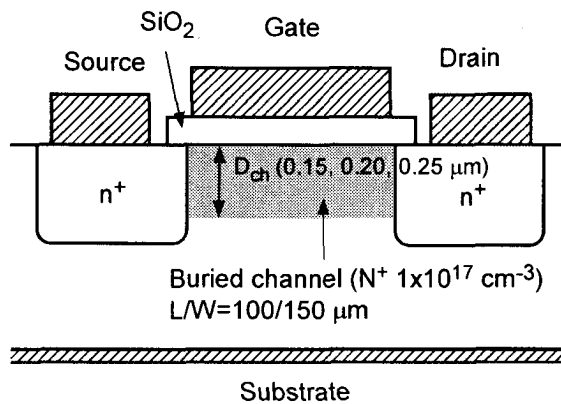


Fig.1. Schematic cross section of a 4H-SiC buried channel MOSFET.

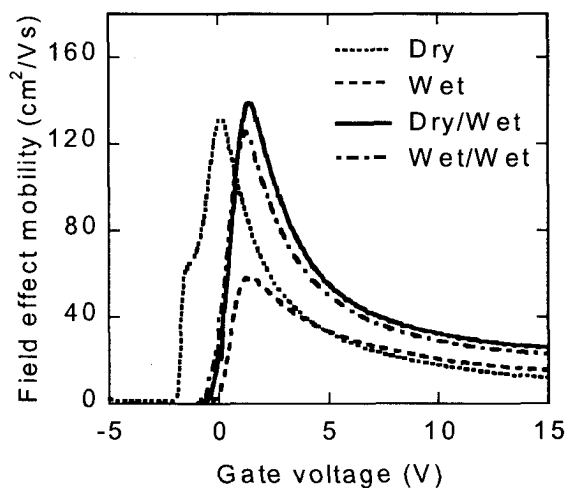


Fig.2. Field effect mobility as a function of gate voltage in the buried channel MOSFETs with the gate oxide processed by different condition. Drain voltage is 0.1V. The depth of the buried channel region and the concentration are 0.2 μm and $1 \times 10^{17} \text{ cm}^{-3}$, respectively.

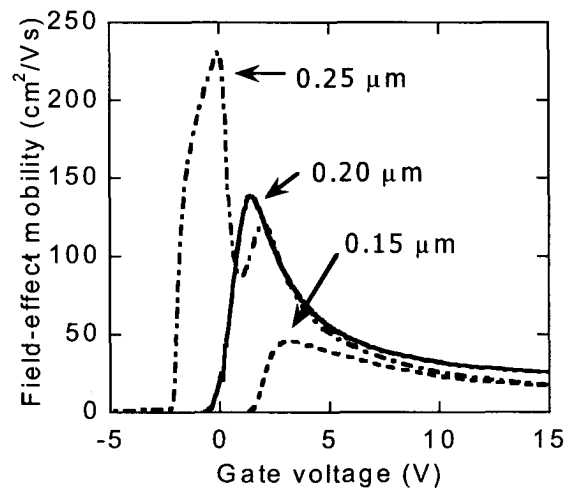


Fig.3. Field effect mobility as a function of gate voltage and depth of the buried channel region. The gate oxide is grown by dry oxidation and following wet re-oxidation.

Channel Engineering of Buried-channel 4H-SiC MOSFET based on the Mobility Model of the Oxide/4H-SiC interface

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In a buried-channel SiC MOSFET, it is indispensable to perform channel engineering by simulation in order to set threshold voltage at an appropriate value and to avoid the mobility fall near a SiC/oxide interface. In the simulation of MOSFET, it is important to set the proper mobility model at a semiconductor/oxide interface. However, the mobility model of a SiC/oxide interface has not been proposed until now. In this study, we modeled the mobility in the vicinity of the SiC/oxide interface, for the first time, from the experimental results of a surface channel SiC MOSFET and a buried-channel SiC MOSFET.

Figure 1 shows the field effect mobility of a surface channel SiC MOSFET. It should be noted that the electric field dependence of mobility is very small. Thus, we assumed that the inversion layer mobility is a constant of $25\text{cm}^2/\text{Vs}$ [1], and the degradation of mobility due to interface decays exponentially as the distance from the interface increases. Figure 2 shows the comparison of an experimental result and a simulation result with this mobility model. In this mobility model, the characteristic length (l_{crit}) of the mobility degradation due to interface is another important parameter. From the experimental results of a buried-channel SiC MOSFET, we try to calibrate l_{crit} , because the simulation results of a surface channel SiC MOSFET are almost independent of l_{crit} . Figure 3 shows the comparison of an experimental result of a buried-channel SiC MOSFET and a simulation result with the optimized l_{crit} of 30nm[2].

With this SiC/oxide interface mobility model, we performed channel engineering of a buried-channel SiC MOSFET. Figure 4 shows an example of an optimized new structure. A p layer is stacked between oxide and buried channel. Figure 5 shows the comparison of a simulation result of a p layer-stacked buried-channel MOSFET with that of a conventional buried-channel MOSFET. It can be seen that a remarkable increase of drain current is obtained in a p layer-stacked buried-channel MOSFET.

This work was performed under the management of FED as a part of the MITI NSS Program (Ultra-Low Loss Power Device Technology Project) supported by NEDO.

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[2] S. Harada et al., to be published in IEEE Electron Device Letters

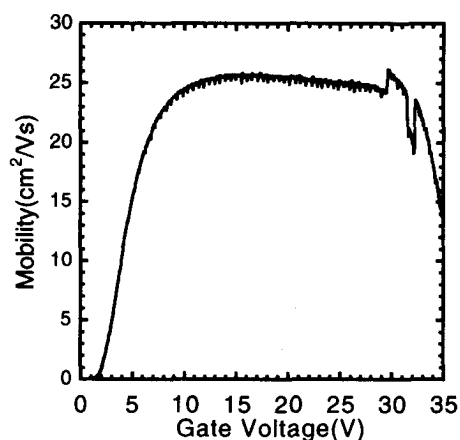


Fig. 1: Field effect mobility of surface channel SiC MOSFET.

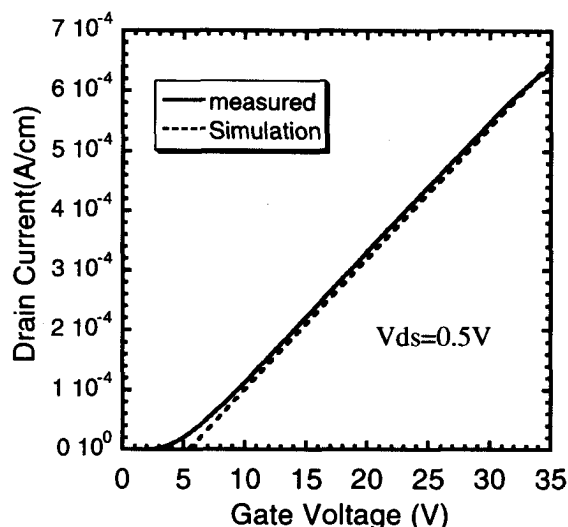


Figure 2: Linear region characteristics for the surface-channel MOSFET. Line shows the measured results and broken line shows simulated results with constant mobility model at the SiC/oxide interface.

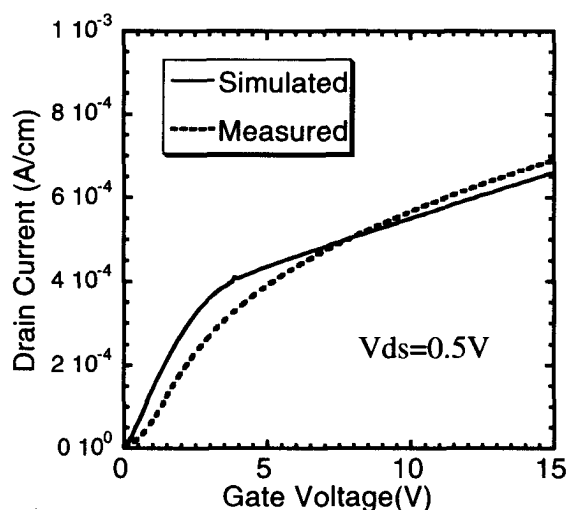


Figure 3: Comparison between the measured results of gate voltage versus drain current characteristics of buried-channel MOSFET and simulated results with optimized mobility model.

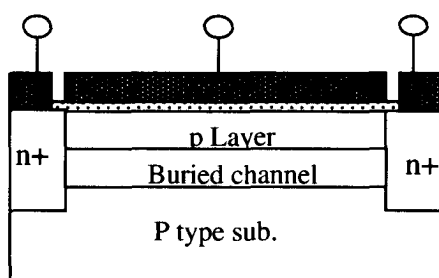


Figure 4: Schematic cross section of p layer- stacked buried-channel MOSFET.

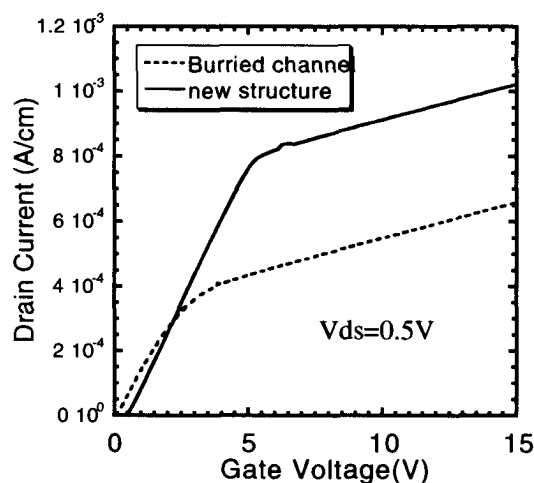


Figure 5: Comparison between the gate voltage vs. drain current characteristics of conventional buried-channel MOSFET and that of p layer-stacked buried-channel MOSFET.

4H-SiC MOSFETs on (03 $\bar{3}$ 8) Face

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The selection of surface orientation is important for fabrication of MOSFETs on 4H-SiC, since a higher inversion channel mobility has been obtained on the (11 $\bar{2}$ 0) face compared to the (0001) face[1]. In general, Si MOSFETs are fabricated on the (001) face, because the lowest density of interface states is obtained on the (001) face. The (0001) and (11 $\bar{2}$ 0) faces of 4H-SiC (hexagonal crystal structure) correspond to the (111) and (110) faces of Si (cubic structure), respectively. The surface orientation which corresponds to the (001) face for the cubic structure is the (03 $\bar{3}$ 8) face of 4H-SiC. 4H-SiC(03 $\bar{3}$ 8) is the face tilted by 54.7° toward $\langle 01\bar{1}0 \rangle$ from 4H-SiC(0001) as illustrated in Fig.1. In this paper, the interface characterization of MOS capacitors and the MOSFET performance on 4H-SiC(03 $\bar{3}$ 8) are reported for the first time.

4H-SiC(03 $\bar{3}$ 8) substrates were prepared by slicing ingots grown by a modified-Lely method on (000 $\bar{1}$) at SiXON Ltd. with an angle of 54.7° toward the $\langle 01\bar{1}0 \rangle$ direction. For comparison, 4H-SiC(0001) substrates were also examined. N-type and p-type epilayers were grown by CVD for fabrication of n-MOS capacitors and inversion-type n-channel MOSFETs, respectively (n-epi; $N_d = 3.1 \times 10^{17} \text{cm}^{-3}$ for (03 $\bar{3}$ 8), $8.9 \times 10^{16} \text{cm}^{-3}$ for (0001), p-epi; $N_a = 9.6 \times 10^{15} \text{cm}^{-3}$ for (03 $\bar{3}$ 8), $1.1 \times 10^{16} \text{cm}^{-3}$ for (0001)). After RCA cleaning, wet oxidation was carried out at 1150°C to grow a thermal oxide followed by in-situ Ar annealing at 1150°C for 30min. The oxidation time and resulting thickness were 25min and 70nm for (03 $\bar{3}$ 8), and 120min and 50nm for (0001), respectively. The oxidation rate on (03 $\bar{3}$ 8) was 6-7 times higher than that on (0001). The gate metal was Al for both MOS capacitors and MOSFETs. The gate length (L) and width (W) of MOSFETs were 50 and 200 μm , respectively.

Figure 2 shows the distribution of interface state density (D_{it}) in n-type MOS capacitors estimated by a conductance method measured at room temperature. Though D_{it} on (03 $\bar{3}$ 8) is larger than on (0001) at relatively deep energy ($E_C - E > 0.4\text{eV}$), MOS capacitors on (03 $\bar{3}$ 8) indicate 3-5 times smaller D_{it} at shallow energy ($E_C - E = 0.1\text{-}0.2\text{eV}$) than on (0001). In high-frequency C - V measurements, when the measurement temperature was cooled down from 300 to 100K, an increase of flatband voltage shift and hysteresis was small for MOS capacitors on (03 $\bar{3}$ 8) while that was large on (0001). This result also revealed smaller D_{it} near the conduction band edge on the (03 $\bar{3}$ 8) face.

All MOSFETs showed clearly the linear region and the saturation region. The drain current (I_D) - gate voltage (V_G) characteristics in the linear region (drain voltage (V_D) = 0.1V) are shown in Fig.3, in which I_D is normalized by the oxide capacitance (C_{ox}) to compare MOSFETs with different oxide thickness graphically. The higher drain current and steeper slope on (03 $\bar{3}$ 8) in Fig.3 suggest that a higher channel mobility was obtained

by using the (03 $\bar{3}$ 8) face instead of (0001) face in 4H-SiC. The threshold voltages determined from the onset of drain current in Fig.3 are also clearly different for both faces. A lower threshold voltage (~ 5 V) was observed for MOSFETs on (03 $\bar{3}$ 8) compared to MOSFETs on (0001) (~ 9 V). Effective mobilities calculated from the slope of I_D - V_G curves in Fig.3 are plotted in Fig.4 as a function of the threshold voltage for corresponding MOSFETs. The maximum low-field mobility was $22\text{cm}^2/\text{Vs}$ for (03 $\bar{3}$ 8) and $5\text{cm}^2/\text{Vs}$ for (0001) samples. The improvement in channel mobility by a factor of 3-5 was achieved by using the (03 $\bar{3}$ 8) face in 4H-SiC. The temperature dependence of MOSFET performance and comparison of MOSFETs on (11 $\bar{2}$ 0) will be presented at the conference.

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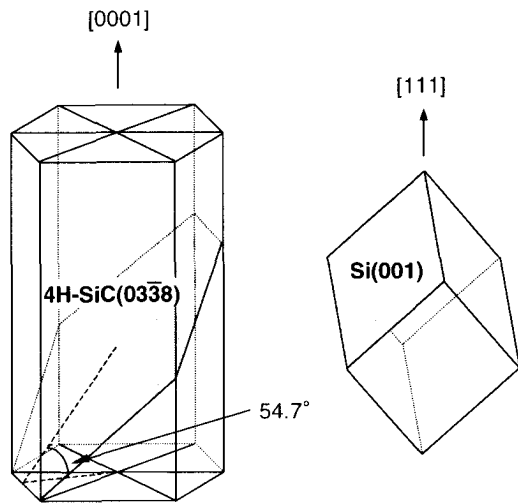


Fig.1: 4H-SiC(03 $\bar{3}$ 8) and Si(001).

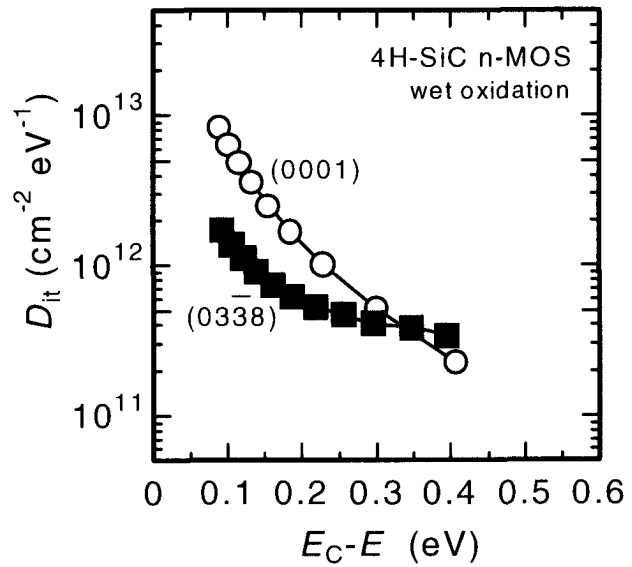


Fig.2: Interface state distributions.

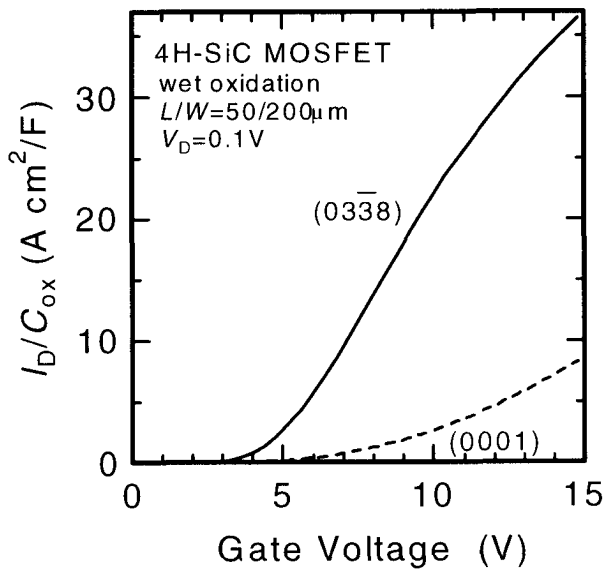


Fig.3: Linear-region I_D - V_G characteristics.

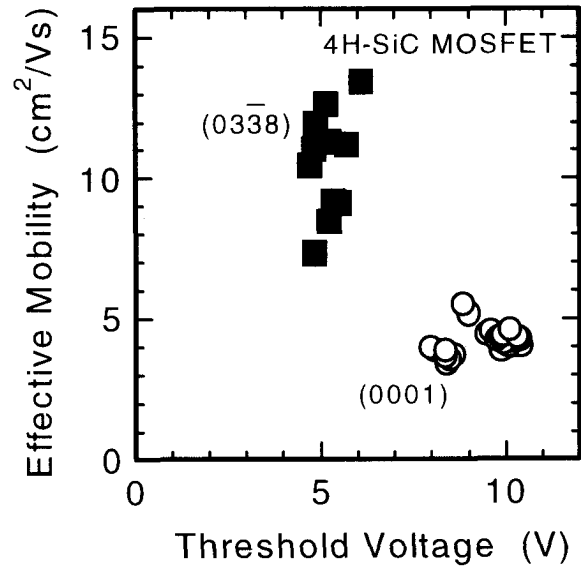


Fig.4: Relation between effective mobility and threshold voltage.

MISiCFET chemical gas sensors for high temperature and corrosive environment applications

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A silicon carbide chemical gas sensor has been under development in a co-operative effort between S-SENCE and ACREO [1-6]. The sensor is based on a field-effect transistor (FET), which was designed and processed by ACREO [1]. The metal insulator silicon carbide field effect transistor, MISiCFET, functions as a gas sensor by the application of catalytic gate metals, Pt, Ir. The device design is shown in Fig. 1. The source and gate of the device are connected to create a convenient two terminal sensor device. A voltage applied between the source and drain contacts causes a current to flow between these contacts through the buried channel region. The catalytic metal is placed over the channel region. Gas molecules in the atmosphere, which react with the gate metal will charge the gate region of the device and hence cause the concentration of mobile carriers in the channel to change. This in turn will shift the IV characteristics in a similar way to that shown in Fig 2. In order to promote high-temperature stability, the source, drain and channel region are buried. This moves the conducting path in the device away from the surface of the SiC, thus reducing the influence of surface effects. Batch number three of the devices has been completed and successfully tested in several applications at temperatures up to 600°C. The devices show excellent stability. Further testing of their performance limits is under way.

We have identified several applications in car exhausts where the excellent properties of SiC are a prerequisite. A cold start sensor needs to tolerate temperatures from -20°C to 1000°C and should even tolerate water splashes at its operation temperature (around 600°C). Promising results have been obtained to date. During Selective Catalytic Reduction of diesel exhausts, NO_x is reduced by NH₃ in the catalytic converter. An ammonia sensor for control of ammonia injection should not be contaminated by particulates and should show very low cross sensitivity to NO_x. The MISiC sensor operated at 300°C has demonstrated very promising results.

In flue gases a sensor array is needed to identify different modes of the combustion in a boiler. It is intended that a prototype version of a sensor system will be constructed, including software for control of the combustion process.

At the conference, typical results from the different applications will be shown.

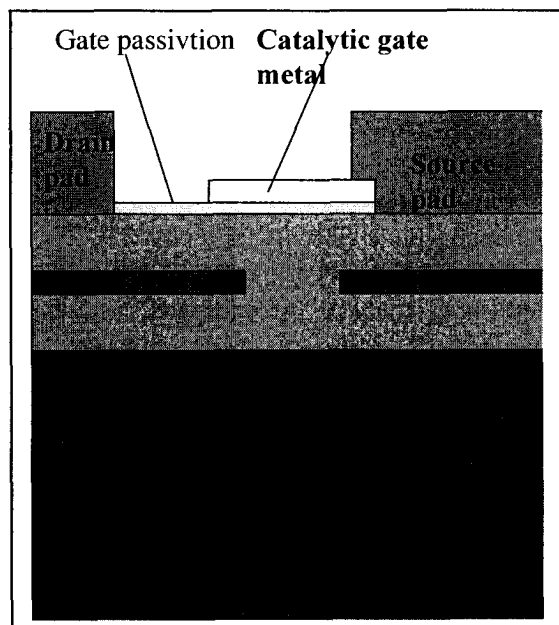


Fig. 1. . Cross-section of silicon carbide FET (MISiCFET) sensor with a buried gate design [1].

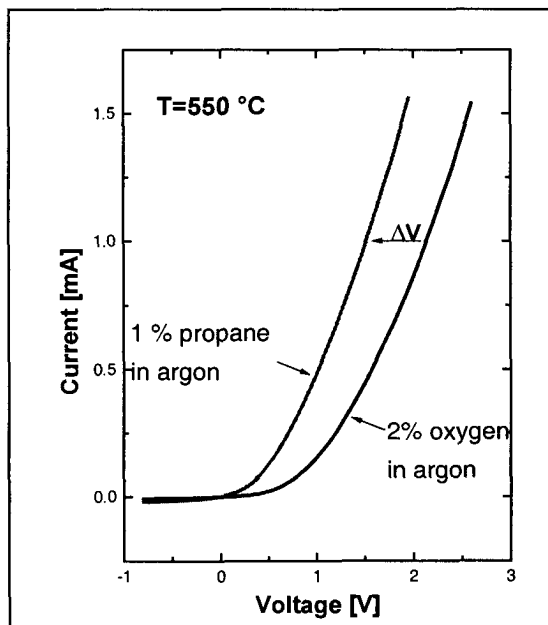


Fig. 2. Current voltage, IV, characteristics of a MISiC sensor. The voltage at a constant current is the sensor signal, which shifts in different gas ambients.

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4H-SiC Material for Hall Effect and High Temperature Sensors Working in Harsh Environment

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Silicon carbide is a well-known material for the fabrication of devices working in harsh environment. In this work we show that this material is also a good candidate to produce magnetic sensors working at high temperature [1].

The electrical properties of n-type, nitrogen-doped, 4H-SiC samples are well-known [2]. Recently we investigated a series of samples grown by AP-CVD, with carrier concentration ranging from $3.5 \times 10^{15} \text{ cm}^{-3}$ to $7.5 \times 10^{17} \text{ cm}^{-3}$. A model was developed, which gives a complete description of the electron density and mobility as a function of temperature in the range 30 K to 900 K and doping concentration 10^{14} cm^{-3} to 10^{18} cm^{-3} .

In the framework of this model, we could determine the doping conditions in which (starting from room temperature) the material is working in the exhaustion regime. To be fulfilled, the doping level has to be lower than $5 \times 10^{15} \text{ cm}^{-3}$. This is shown in Fig. 1.

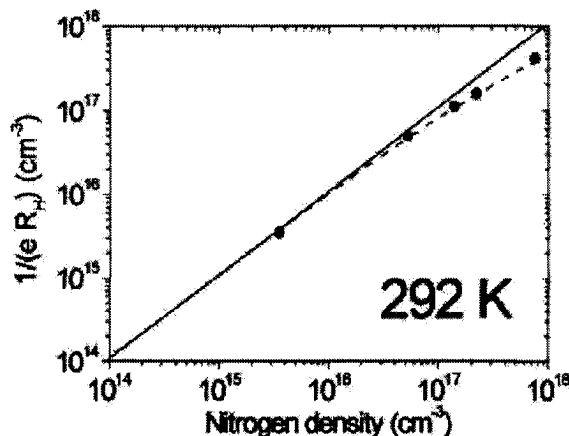


Figure 1: Hall electron density versus donor density.
Full line - total ionization, dashed line - calculated values at 292 K,
full circle - experimental data

As prototype sensor, we have used a sample with $2.4 \mu\text{m}$ thick active layer doped at a concentration of $3.5 \times 10^{15} \text{ cm}^{-3}$. The magnetic field sensitivity $K_H = 1/(N_s \times e)$, in which N_s is the sheet carrier density, is $K_{H0} = 930 \text{ V/A/T}$ at room temperature. The temperature sensitivity S_T is only $+75 \text{ ppm/K}$ between 300 K and 550 K and -500 ppm/K between 550 K and 800 K (see Fig. 2). Such small values present a great advantage since no compensating circuit for thermal drift is needed for high temperature applications. They compare well with the one (-140 ppm/K) achieved in the case of metrology-type magnetic sensors based on III-V heterostructures between 230 and 380 K. Such stable structures with a GaAlAs/GaInAs/GaAs stacking are actually used for electrical metering applications[3].

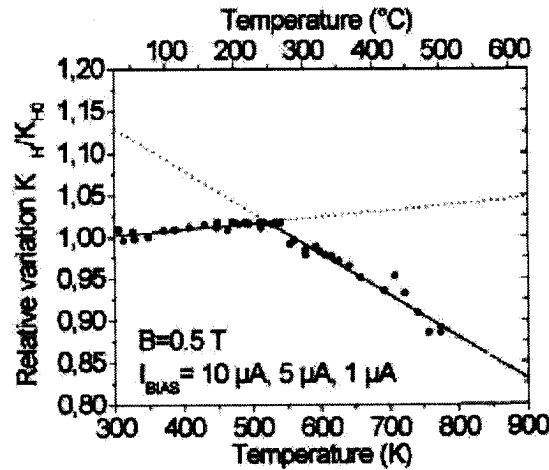


Figure 2 : Relative variation of the sensitivity K_H/K_{H0} of the sensor (experimental data – full circles). Lines show the thermal drift (between 300–500 K: $S_T = +75$ ppm/K, between 500–800 K: $S_T = -500$ ppm/K).

When additional temperature knowledge is required, a bridge shape geometry can be used and, in this case, the input resistance of the device acts as a temperature sensor. In Fig. 3, we show the temperature dependence of the sheet resistance. The temperature sensitivity is equal to +3400 ppm/K between 500K and 800K.

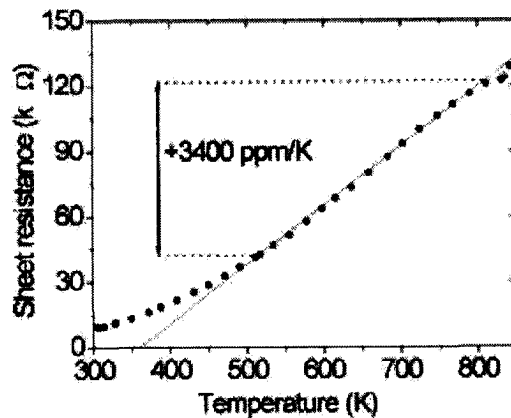


Figure 3: Variation of the sheet resistance versus temperature.
The thermal sensitivity of the sheet resistance is +3400 ppm/K between 500 – 850 K.
The solid line is a linear fit in this temperature range.

As a result, using a well-suited geometry, we have found that the same component can be used for magnetic field and temperature measurements. Such monolithic structure avoids systematic errors introduced by temperature gradients inevitable when using two separated sensors.

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High Temperature performance of 10 Kilovolts, 200 Amperes (Pulsed) 4H-SiC PiN Rectifiers

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SiC is a superior material system for the fabrication of ultra high voltage devices since it is capable of sustaining a very high power density, which can be switched at an extremely high speed, while operating at very high temperatures. Such diodes would be suitable for solid state power conditioning systems for high power radar, directed energy weapons, X-ray generators, electrostatic precipitators and high power LASERS. This paper reports the highest power single chip 4H-SiC PiN rectifier demonstrated to date, with a 2 MegaWatt (Pulsed) capability.

These diodes had an active metallized Anode area of approximately 0.09 cm^2 (3mm X 3mm). A high purity, $150 \text{ }\mu\text{m}$ n^- epitaxial layer doped at $7\text{E}14 \text{ cm}^{-3}$ was used in the fabrication of these rectifiers. This voltage-blocking layer was grown using a refined hot wall CVD growth reactor yielding low epi defect densities. The highly doped, $1.8 \text{ }\mu\text{m}$ p^+ Anode was grown epitaxially in order to obtain good carrier injection during on-state operation. To prevent premature breakdown, the voltage blocking layer was exposed using reactive ion etching, and a $400 \text{ }\mu\text{m}$ wide, optimized Junction Termination Extension (JTE) was implemented using a p-type implant at the periphery of the device edge. The SiC surface at the edges were then passivated using a thick SiO_2 layer. This termination allowed a 10 kV blocking capability with a leakage current of only $20 \text{ }\mu\text{A}$ for these 3mm X 3mm diodes. Measurements conducted up to 200°C and 3 kV show practically no change in the leakage current using our measurement system with a $3 \text{ }\mu\text{A}$ sensitivity. Measurements at higher voltages will be presented at the conference.

The forward characteristics were found to be fairly uniform on rectifiers fabricated throughout the wafer, with most rectifiers turning on close to the built-in voltage (2.9 to 3 V) of 4H-SiC. Thereafter, these rectifiers have a much steeper I-V slope as compared to Si diodes. At room temperature, pulsed measurements using a high power curve tracer shows that the forward voltage drop was 4.5 V at 100 A/cm^2 (10 A); 7.07 V at 500 A/cm^2 (45 A); and only 12.5 V at 2200 A/cm^2 (200 A). On-state measurements conducted in the room temperature to 200°C temperature range (in 50°C intervals) show a slight reduction in on-state voltage drop from 7.2 V to 6.9 V at 50 A on this packaged device.

These rectifiers show fairly stable reverse recovery switching characteristics as the operating temperature was increased from 25°C to 200°C . A forward current of 20 A (220 A/cm^2) was switched at a reverse dI/dt of $120 \text{ A}/\mu\text{sec}$ with an applied reverse voltage of 100 V. At room temperature, the peak reverse recovery current of only 8.7 A was observed and the device turned off completely within 600 nsec. This complete turn-off time increases to $1 \text{ }\mu\text{sec}$ at 200°C under similar test conditions. The peak reverse recovery increases a modest 72% to 15 A between room temperature and 200°C .

Wafer maps showing the distribution of on-state voltage drop and blocking voltage show fairly good yields when a criteria of $>7 \text{ kV}$, 4.5 V (100 A/cm^2) is used. These data and the details of high temperature measurements will be presented at the conference.

This work is supported in part by Wright Labs under DUS&T Technology Investment Agreement number F33615-01-2-2108, monitored by Jim Scofield.